SGS-THOMSON MICROELECTRONICS

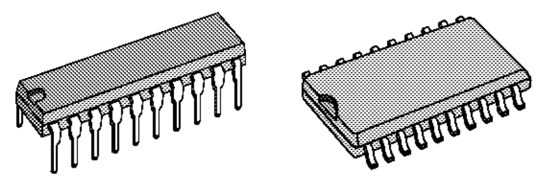
L6372

OCTAL INDUSTRIAL INPUT INTERFACE

PRODUCT PREVIEW

- INPUT STATUS MONITORING BY MEANS OF CURRENT LEVELS DETECTION
- EXTERNALLY PROGRAMMABLE UPPER CURRENT LEVEL
- INPUT OPEN LINE DETECTION
- INPUT PROTECTION BY MEANS OF INTERNAL DIODES CLAMPING TO GROUND AND SUPPLY VOLTAGE
- DIGITAL FILTERING OF NOISE ON EACH CHANNEL
- ALLOWS IMPLEMENTATION WITH MINIMUM POWER DISSIPATION OF 8 CURRENT SINKING INPUTS ACCORDING TO THE IEC STANDARD
- DATA TRANSFER FROM PARALLEL IN TO SERIAL OUT

MULTIPOWER BCD TECHNOLOGY



POWERDIP 16+2+2 SO 16+2+2

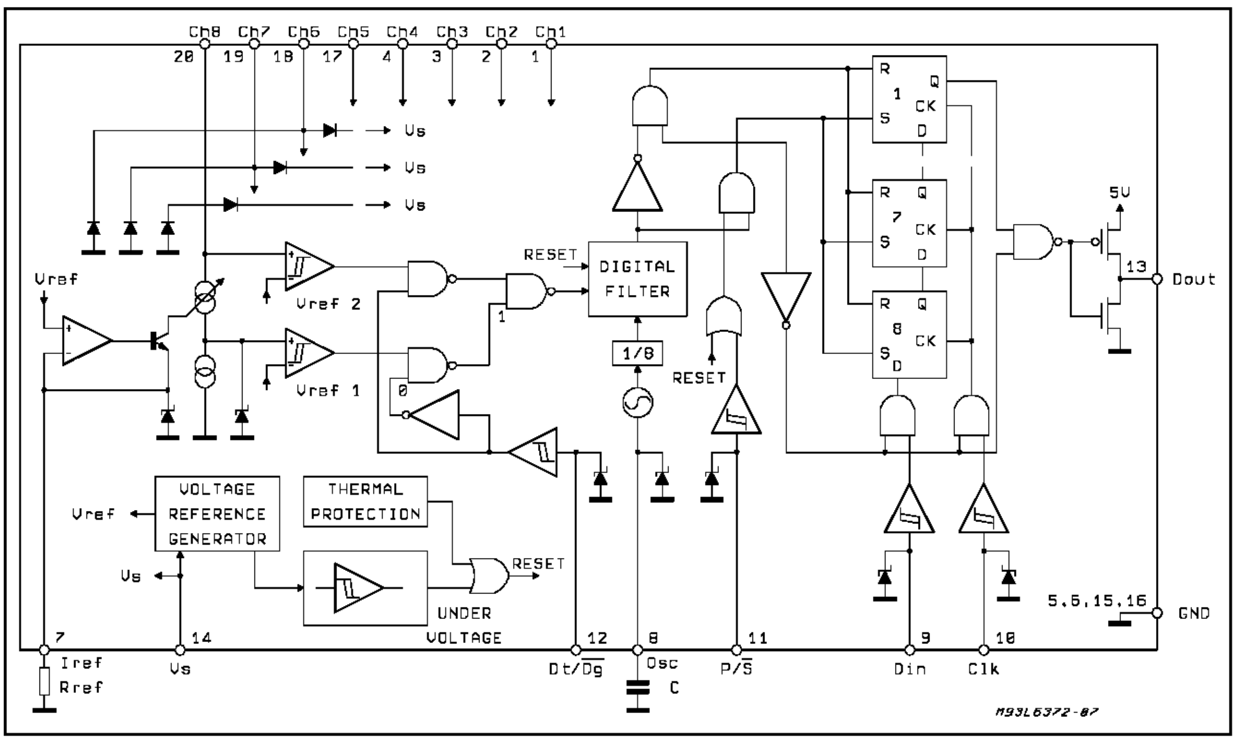
ORDERING NUMBERS: L6372DP (Powerdip16+2+2)
L6372FP (SO16+2+2)

DESCRIPTION

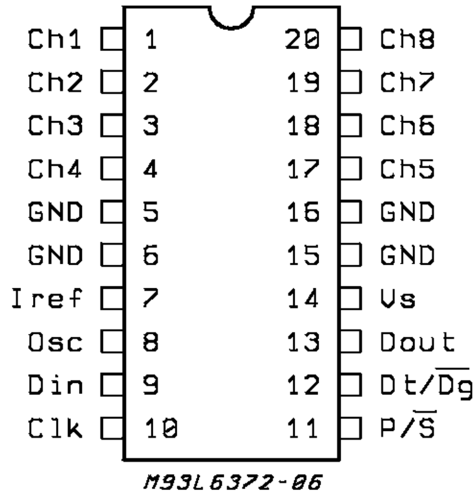
The L6372 is especially designed for use as a line receiver in industrial control systems based on the 24V/6mA signal levels (IEC1131, 24VDC, type 2). 8 input lines can be connected to the device.

Up to 8 input lines can be connected to each device. Several devices can be linked to monitor more than 8 lines.

FUNCTIONAL DIAGRAM



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
V_S	14	Supply Voltage ($t_W \le$ 10ms)	40	V
V_{Ilog}	9	Logic Input Voltage (DC)	-0.3 to 7	V
	10	(see channel Protection)		
I_{Ilog}	11, 12	Logic Input Forced Current, per pin	±1	mA
I_I	1, 2, 3, 4, 17, 18, 19, 20	Channel Input Current ($t_W \le$ 1ms) (see channel Protection)	±2	A
$V_{line - i}$		Channel Input Voltage (see channel Protection)	-0.3 to V_S +0.3	V
I_{out}	13	Output Current	10 to -20	mA
V_{out}		Output Voltage	-3 to 5	V
I_{set}	7, 8	Setting pins Forced Current	±1	mA
V_{set}		Setting pins Forced Voltage	- 0.3 to 5	V
T_{op}		Ambient Temperature Operating Range	- 25 to 85	°C
T_j		Junction Temperature Operating Range (see Overtemperature Protection)	- 25 to 125	°C
T_{st}		Storage Temperature Range	- 55 to 150	°C

Note: ESD immunity for pins 1,2,3,4,17,18,19 and 20 is guaranteed up to 1200V (Human Body Model–Negative spike versus V_S)

ELECTRICAL CHARACTERISTICS (T_j = -25 to 125°C; V_S = 24V; unless otherwise specified.)
DC OPERATION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	14	Supply Voltage	(operative)	12	24	35	V
V_{sh}	14	Power-on Upper Threshold	V_S Variable	9.8	10.4	11	V
$V_{S\ Hys}$	14	Power-on Hysteresis		400	800	1600	mV
I_S	14	Supply Current	V_S = 12 to 35V T_j = -25°C All Inputs I_i = 1mA, V_S = 24V		12		mA
			V_S = 12 to 35V T_j = 25°C All Inputs I_i = 1mA, V_S = 24V		10.5		mA
			V_S = 12 to 35V T_j = 125°C All Inputs I_i = 1mA, V_S = 24V		9		mA
V_{oh}	13	Output Voltage High	I_O = 0; V_S = 12 to 35V	4.8	5.2	5.5	V
			I_O = 3mA; V_S = 12 to 35V	3.5			V
I_{oh}	13	Output Source Current	V_O = 2V; V_S = 12 to 35V	4			mA
V_{ol}	13	Output Voltage Low	I_O = 4mA; V_S = 12 to 35V			0.4	V
			V_S = 24V; T_j = 25°C		0.15		V
I_{ol}	13	Output Sink Current	V_O = 5V; V_S = 12 to 35V	5			mA
			V_S = 24V; T_j = 25°C		12		mA
V_{th+} (*)	9 to 12	Positive Going Input Threshold	V_S = 12 to 35V	1	1.3	1.6	V
V_{th-} (*)	9 to 12	Negative Going Input Threshold	V_S = 12 to 35V	0.85	1.1	1.4	V
Hy_{in} (*)	9 to 12	Input Hysteresis	V_S = 12 to 35V	0.1	0.2	0.4	V
I_{lin}	9 to 12	Input Leak Current	V_S = 12 to 35V; V_{in} =-0.2 to 5.2V	-100		100	μA
I_1	1 to 4, 17 to 20	Limited Input Current	V_I = 0.5 to 1.1V	0.375	0.550	0.750	mA
I_2	1 to 4, 17 to 20	Limited Input Current	R_{ref} = 12KΩ; V_{in} = 2.4 to 30V I_2 appr. = $K_2 \bullet$ 1.26V/R_{ref} for R_{ref} = 11 to 30KΩ	6.1	6.8	7.48	mA
V_{reg}	1 to 4, 17 to 20	Regulated Input Voltage	I_I = 0.750 to 2mA	1.0	1.2	1.6	V
			I_I = 2 to 6.1mA	1.0	1.2	2.4	V
V_{1l}(*)	1 to 4, 17 to 20	Comparator 1 Low Threshold		0.4	0.7		V
V_{1h} (*)	1 to 4, 17 to 20	Comparator 1 High Threshold			0.9	1.0	V
H_{c1} (*)	1 to 4, 17 to 20	Comparator 1 Hysteresis		0.1	0.2	0.4	V
V_{2l}	1 to 4, 17 to 20	Comparator 2 Low Threshold		1.6	2.0		V
V_{2h}	1 to 4, 17 to 20	Comparator 2 High Threshold			2.2	2.4	V
H_{c2}	1 to 4, 17 to 20	Comparator 2 Hysteresis		0.1	0.2	0.4	V

(*) Guaranteed by design, not tested.

ELECTRICAL CHARACTERISTICS (T_j = -25 to 125°C; unless otherwise specified.)

AC OPERATION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{osc} (*)	Oscillator Frequency	C = 1.2nF; R_{ref} = 12KΩ;	8.8	10	11.2	kHz
I_{chg} (*)	Current Charging	R_{ref} = 12KΩ	40	50	60	µA
V_{hosc}	Upper Switching Threshold			3.2	3.7	V
V_{losc}	Lower Switching Threshold,		1	1.5		V
t_{sv}	Time Serial Valid	Time from 0.85V on pin P/$\overline{S}$ to the first rising edge of the external clock	0.8			µs
t_{so}	Time Serial Out	Time from negative edge on pin P/$\overline{S}$ to activation of the output buffer of D_{out} with the content of the eighth flip/flop			0.35	µs
t_{ckh}	High Level Clock Duration		300			ns
t_{ckl}	Low Level Clock Duration		300			ns
F_{clock}	Clock Frequency				1.5	MHz
t_r	Clock Rise Time				500	ns
t_f	Clock Fall Time				500	ns
t_{su}	Set up Time for D_{in} before the Clock Rising Edge		200			ns
t_{hold}	Hold Time for D_{in} after the Rising Edge of the Clock		0			ns
t_{delay}	Delay Time of D_{out} after the rising Edge of the Clock		15	45	150	ns
τ_{pdin}	Internal Delay, D_{in} to the D Input of the First of the Eight Flip/Flops		50	90	200	ns

(*) F_{osc} and I_{chg} vary inversely to R_{ref}, for R_{ref} from 11KΩ to 30KΩ.

THERMAL DATA

Symbol	Parameter	DIP 20	SO 20	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction to Pin	12	17	°C/W
$R_{th\ j\text{-}amb\ 1}$	Thermal Resistance Junction to Ambient (see Thermal Characteristics)	40	65	°C/W
$R_{th\ j\text{-}amb\ 2}$	Thermal Resistance Junction to Ambient (see Thermal Characteristics)	50	80	°C/W

THERMAL CHARACTERISTICS

$R_{th\ j\text{-}pin}$

POWERDIP. The thermal resistance is referred to the thermal path from the dissipating region on the top surface of the silicon chip, to the points along the four central pins of the package, at a distance of 1.5 mm away from the stand-offs.

SO. Similarly, the reference point is the knee on the four central pins, where the pins are upwardly bent and the soldering joint with the PCB footprint can be made.

$R_{th\ j\text{-}amb\ 1}$

If a dissipating surface, thick at least 35µm and with a surface similar or bigger than the one shown, is created making use of the printed circuit. Such heatsinking surface is considered on the bottom side of an horizontal PCB (worst case).

$R_{th\ j\text{-}amb\ 2}$

If the power dissipating pins (the four central ones), as well as the others, have a minimum thermal connection with the external world (very thin strips only) so that the dissipation takes place through still air and through the PCB itself.
It is the same situation of point above, without any heatsinking surface created on purpose on the board.

Additional data for the PowerDip package can be found in:
Application Note 9030:
Thermal Characteristics of the Power Dip 20, 24 Packages Soldered on 1,2,3 oz. Copper PCB

Figure 1: Printed Heatsink

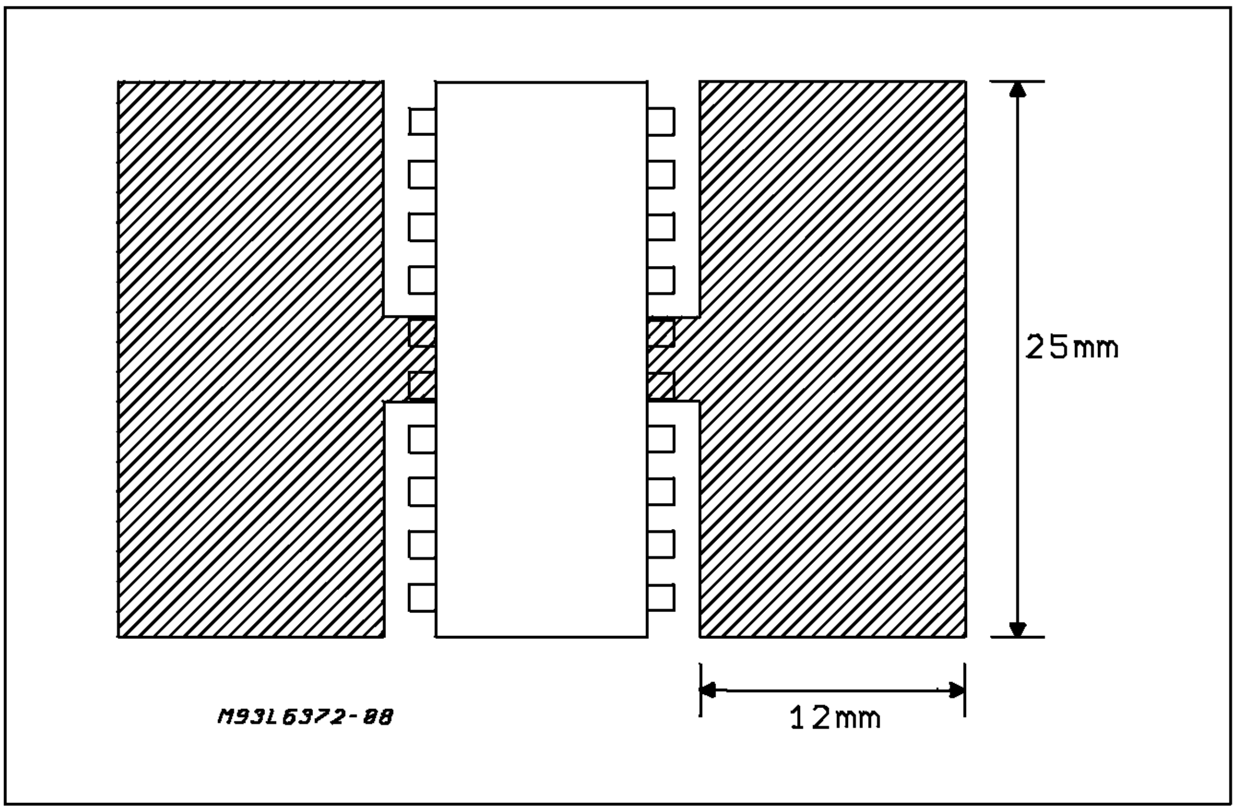
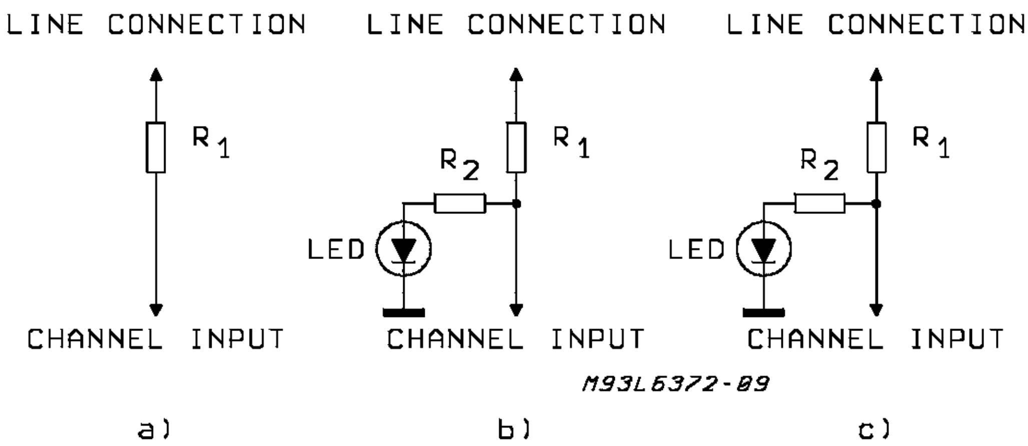


Figure 2: External Channel Circuits



	R_{ref}	R_1	R_2	Vs
case a	12 KΩ ±2%	1.1KΩ ±5%	—	12 to 35V
case b	15 KΩ ±2%	1.0KΩ ±5%	2.0K Ω ± 5%	11.6 to 12V
case c	18 KΩ ±2%	1.2KΩ ±5%	680 Ω ± 5%	12 to 35V

EXTERNAL LINE CHARACTERISTICS

The input characteristics of each of the eight channels of the L6372 do not implement directly the input characteristics required by the "IEC1131, 24VDC, type 2", because the IEC specification requires that the line receiver uses at least a certain amount of power, that is, for eight inputs, more than the maximum power that a silicon IC in a package of reasonable dimensions can dissipate.

The solution adopted includes one or two external resistors per every line receiver implemented. One resistor is sufficient if no visual indication of the line status is required. If a LED is included, two resistors are sufficient, and in addition the channel input protections of the L6372 also protect the LED.

Different input characteristic; of the line receiver can be implemented according to the choice of the values of

- R_1 (one per input)
- R_2 (if used, one per input)
- R_{ref} (one per IC).

Different input characteristics may be chosen to match the constraints of:

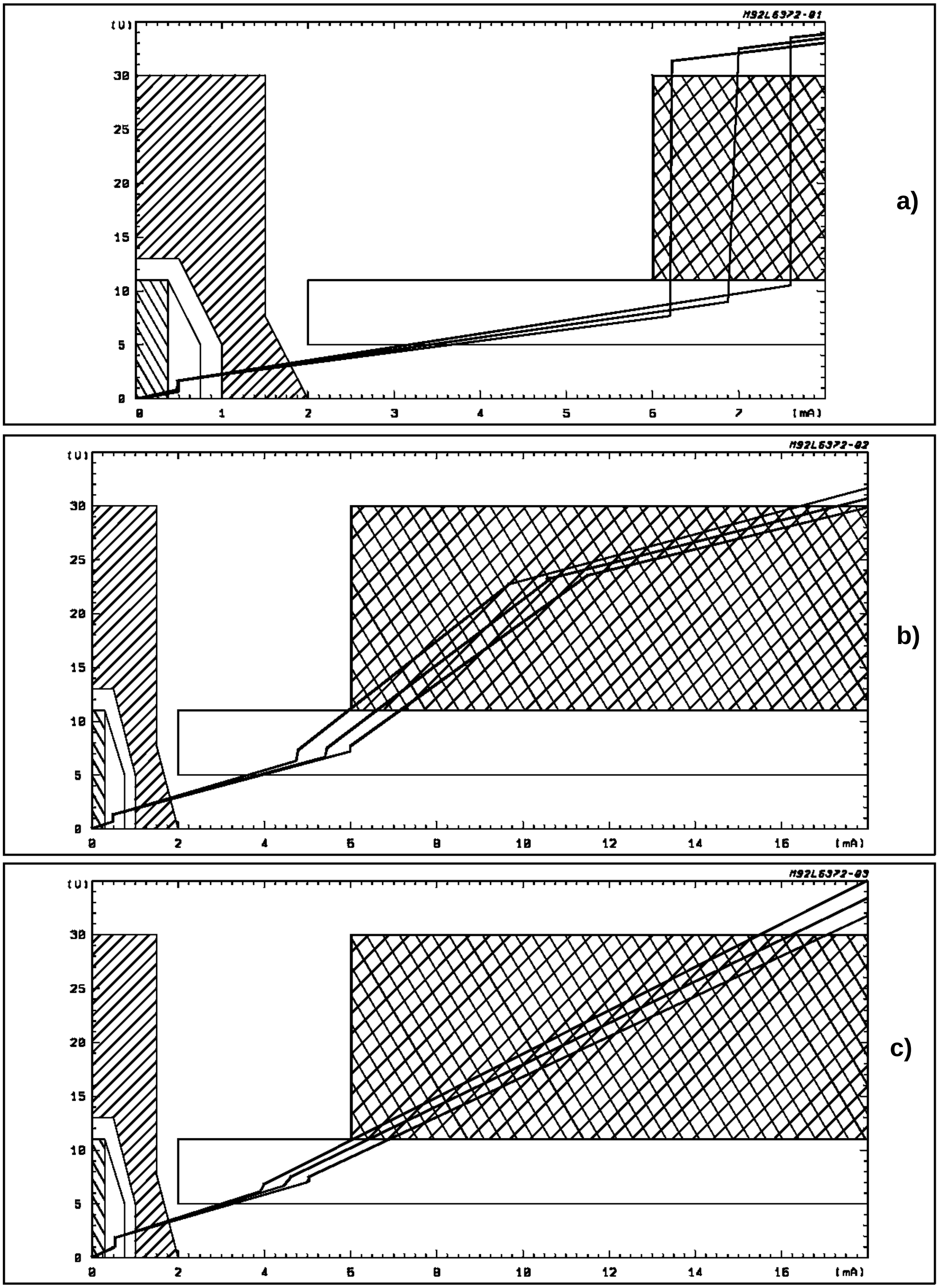
- complying with the mask allowed for the input characteristics by the IEC recommendation (see figure 4);
- not exceeding the maximum allowed power dissipation per line input (depending on the equipment construction and characteristic);
- not exceeding the maximum allowed power dissipation per channel input in the IC (depending upon the type of IC package – DIP or SO – its heatsinking characteristics through the PCB, and the maximum ambient temperature around it).

a) Is the simplest possible case: no visual indication of the line status is implemented; the system dissipation is the minimum possible, but the dissipation in the IC channel is higher than in the cases b) and c).

b) Assumes that V_s can be kept at 12V, and made sink the excess line current from the channel protection diodes when the input lines are at their high level; the channel dissipation can be kept to a minimum.

c) Allows a very low power dissipation, with the LED and V_s anywhere in the allowed range. In all cases the IEC mask is respected because the detection of the transition from "low level received" to "high level received", operated by the thresholds V_{2l} and V_{2h} (see figure 5), takes place when the line voltage is inside the area from 5 to 11 V allowed by the IEC recommendation.

Figure 3


M92L6372-01
(V)
30
25
20
15
10
5
0
0 1 2 3 4 5 6 7 (mA)
a)
M92L6372-02
(V)
0 2 4 6 8 10 12 14 16 (mA)
b)
M92L6372-03
(V)
0 2 4 6 8 10 12 14 16 (mA)
c)

In the following tables the conditions of power dissipation for the three cases are given.

For the calculation of the dissipated power, the extreme case when all channel are working with maximum current, maximum line voltage and maximum supply voltage to the IC (unless otherwise specified) has been considered.

a)

	Min.	Typ.	Max.	Unit
I_{line-i} @ V_{line-i} = 11V	6.12	6.80	7.48	mA
I_{line-i} @ V_{line-i} = 30V	6.12	6.80	7.48	mA
$P_{diss\ on\ chip\ @}$ V_{line-i} = 30V	1.45	1.56	1.65	W
$P_{diss\ on\ board\ @}$ V_{line-i} = 30V	1.79	1.96	2.11	W

b) (V_S = 12V)

	Min.	Typ.	Max.	Unit
I_{line-i} @ V_{line-i} = 11V	6.03	6.60	7.19	mA
I_{line-i} @ V_{line-i} = 30V	16.40	17.22	18.10	mA
$P_{diss\ on\ chip\ @}$ V_{line-i} = 30V	634	698	760	mW
$P_{diss\ on\ board\ @}$ V_{line-i} = 30V	3.39	3.59	3.81	W

c)

	Min.	Typ.	Max.	Unit
I_{line-i} @ V_{line-i} = 11V	6.04	6.47	6.92	mA
I_{line-i} @ V_{line-i} = 30V	15.50	16.39	17.35	mA
$P_{diss\ on\ chip\ @}$ V_{line-i} = 30V	686	725	764	mW
$P_{diss\ on\ board\ @}$ V_{line-i} = 30V	4.07	4.28	4.51	W

The masks in figure3 for the cases a), b), c) plot, in a I/V diagram (horizontally the line input current and vertically the line input voltage), the resulting line input characteristics. They appear as three curves for each diagram, starting from the origin and running close to each other. One shows the case where all tolerances combine to generate the typical case, and the other two to generate the opposite extreme characteristics. In the plots the boundaries of the regions recommended by the "IEC 1131 24VDC, type 2" for the different input decoding functions to take place, are shown.
Other choices for R_1, R_2 and R_{ref} are of course possible, and case by case the set of values shall be different, according to the different design constraint of the application. In the above paragraph it has been assumed that the LEDs are of the green or yellow types (higher forward drop than the more common red ones).

CHANNEL PROTECTION

At the input of each channel, two diodes clamp the voltage to V_s and to ground. They have been designed and sized in order to:

- exhibit a low forward voltage drop when pulses of inrushing current up to 2A are forced, V_f typical of 2V @ 2A (2A corresponds to a voltage of 2KV if a resistor of 1KΩ is put externally in series to each channel input);
- avoid interference of noise pulses on the adjacent channels (a 1A pulse lasting up to 100µs won't be felt in the adjacent channels);
- avoid interference with the overall chip operation due to parasitic elements in the integrated circuit structure (very low leakage to the chip substrate during forward conduction, and no parasitic transistors with the other diffused structures close by in the chip).

The series resistance R_1 combines with the two protection diodes at each channel input, to implement an effective protection from any line disturbance.

INPUT CHANNEL

On each of its 8 inputs the L6372 continuously monitors, by means of two comparators, whether:

- it is possible to sink the high level current (equal to or greater than the level programmed by an external resistor R_{ref}, called I_2 and typically set at 6.8 mA); or
- if at least it is possible to sink a current equal to, or greater than the low level current (fixed inside the IC, called I_1 and having a typical value of 550µA).

If not even the low level current I_1 can be sunk, then the signal is interpreted as " input disconnected ". Around I_1 the input characteristic is a constant current line, and the voltage varies rapidly.

A voltage comparator is sensing the input, and is triggered at levels of V_{1l} (typically 0.7V) and V_{1h} (typically 0.9V). The distance between the two thresholds (hysteresis) is provided to give immunity against the noise that may affect the input signal.

If an intermediate level is detected, sinking a current between I_1 and I_2, the signal is interpreted as "line connected, with a low level signal received".

Again, an internal voltage comparator is used, with two thresholds separated by an hysteresis for noise immunity (V_{2l}, typically 2V and V_{2h}, typically 2.2V). If a level clearly corresponding to the current I_2 is detected, then the signal is interpreted as " line connected, with a high level signal received ".

DATA/DIAGNOSTIC

The signal on pin 12, Dt/$\overline{Dg}$, decides whether the information on the signals level or the information on the status of the lines is transferred to the digital section of the device.

A high level on this pin means that Data are to be transferred to the inputs of the digital filters; a low level means that the Diagnostics are requested instead.

Table 1: Dt/$\overline{Dg}$ selection: input to the digital filter

	INPUT CURRENT (Input Voltage Vi)		
	Below Low Level ($V_i < V_{1l}$)	Between Low and High Level ($V_{ih} < V_i < V_{2l}$)	Above High Level ($V_{2h} < V_i$)
Dt / $\overline{Dg}$ = 0	0	1	1
Dt / $\overline{Dg}$ = 1	0	0	1

At this point one digital filter on each of the eight channels processes the information to suppress the noise. The sampling frequency is externally programmable with combination of the capacitor C and the resistance R_{ref}.

DIGITAL FILTERS
General Function

The digital filter, on each channel, filters out the disturbances of short duration.

Before the signal enters the digital circuitry, a low pass effect of approximately 1.5µsec (low pass below 700kHz) is found in the comparators that perform the analog-to-digital conversion of the input signals.

The signal (Data or Diagnostic according to the choice made by the Dt/$\overline{Dg}$ input signal) is sampled at a fixed frequency.

Such frequency is the frequency of the on-chip oscillator (or of an external signal), divided by 8.

Figure 4: Input Characteristics at Low Levels

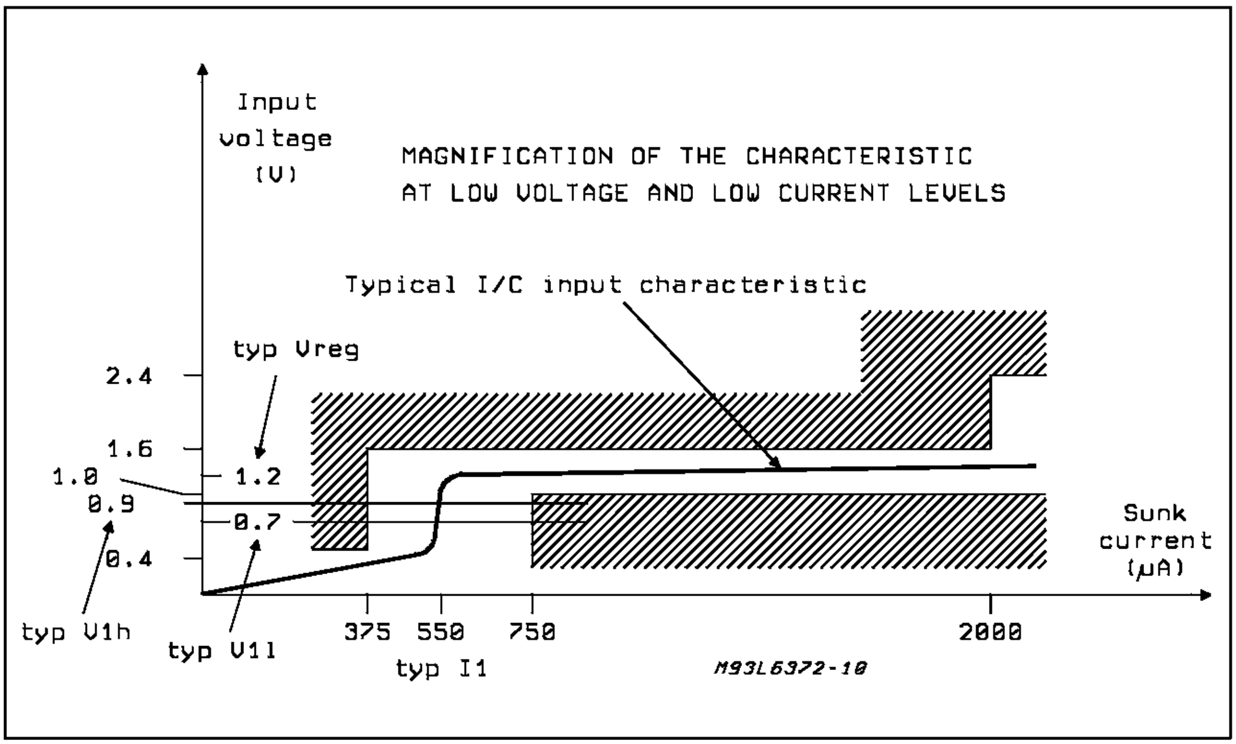
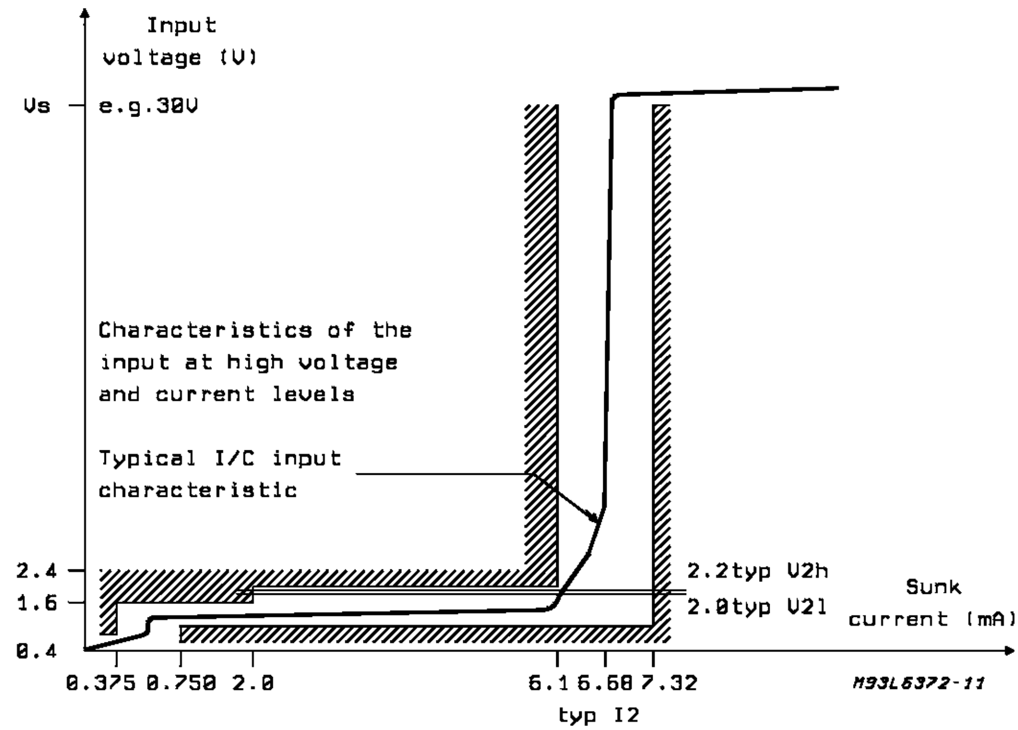


Figure 5: Input Channel Characteristics



Frequency Generation

- Internal

If the local oscillator is used, the pin Osc will be connected to a capacitor C, grounded on the other side.

The oscillation is achieved by an internal current generator, that repeatedly charges and discharges the capacitor C between two voltage levels (V_{hosc} and V_{losc}, typically 3.5V and 1.5V). The current has the same absolute value (I_{chg}) both during the charge and discharge phase.

I_{chg} is obtained mirroring the current that flows through R_{ref} (1.26V/R_{ref}),with a coefficient of 0.457, so that, for instance, if R_{ref} is 12KΩ, I_{chg} is typically 50µA.

The frequency can be calculated as:

$$F_{osc} = \frac{I_{chg}}{2 \cdot C \cdot (V_{hosc} - V_{losc})}$$

For instance, if R_{ref} = 12KΩ and C = 1.2nF, F_{OSC} is about 10KHz.

The method to determine F_{OSC} indicated here above gives the value to be expected with the highest probability. All the positive causes of deviation in the chip, including V_S and T_j, will not, in practice, combine and create a deviation, from such calculated F_{OSC} value, in excess of ±12%.

- External

If an external signal is to be used, it will be fed directly into the Osc pin, without any capacitor for oscillation purposes. The internal impedance of the generator of such signal must be low enough to override I_{chg}, and the voltage swing must exceed the upper (V_{hosc}) and lower (V_{losc}) thresholds. In order to have a margin, add 20% to the I_{chg} value calculated with the formula

$$I_{chg} = \frac{(0.457 \cdot 1.26V)}{R_{ref}}$$

and use for V_{losc} and V_{hosc} the extreme values given in the data sheet.

Filter Operation

Each filter is a synchronous state machine, with 8 significant states, clocked by the oscillator frequency divided by 8.

In 4 states (0XX) the output is 0, in the other 4 states (1XX) the output is 1.

At the chip start-up (power-on reset) or in case of overtemperature the fundamental 0 state is forced (it corresponds to the reset of the filter state).

When the normal operation of the chip is allowed, the input to the filter generates the following transition table:

Present State	Filter Output	Input	Next State
000	0	0	000
000	0	1	001
001	0	0	000
001	0	1	010
010	0	0	000
010	0	1	011
011	0	0	000
011	0	1	100
100	1	0	101
100	1	1	100
101	1	0	110
101	1	1	100
110	1	0	111
110	1	1	100
111	1	0	000
111	1	1	100

It can be seen, for instance, that pulses of the input, with a polarity opposite to the output and lasting for less than four clock periods, are completely filtered out.
If instead the input exhibits a change of level that lasts long enough for four clock edges to sample it, then the output of the filter, after the four clock periods, follows the change of level at the input.
If an input signal with changes that do not occur more often that every 32 periods of the main oscillation is considered, it can be seen that such filter introduces a delay of the input transitions that is randomly variable from 24 to 32 periods of the main oscillation.
In the case of input transitions that occur closer to each other than 24 periods of the oscillator, the resulting pulse is considered an unwanted noise pulse and is consequently eliminated by the filter.
An input pulse lasting between 24 and 32 periods could either be cancelled or acknowledged by the filter, with the delay said above, according to the relative phase of such pulse with respect to the square wave (clock/8) that clocks the filter.

DEVICE OUTPUT

To extract the information from the L6372 (line levels or line statuses according to the Dt/$\overline{\text{Dg}}$ pin) the external processor activates the following sequence:

1) The level on pin P/$\overline{\text{S}}$ (Parallel active high / Serial active low) is brought from its normal high level to a low logical level.
   The parallel jam inputs to the 8 flip-flops of the shift register are disabled. The last datum available is kept in each cell.
   The output of the first cell of the shift register is made available on the output pin Dout. When the L6372 is in parallel mode, Dout is kept at its low level, irrespectively of the output of the shift register.
   The signals on the L6372 inputs Clk and Din are made available on the relevant internal inputs to the shift register.

2) The external processor can now start clocking the shift register.
   At every rising edge of the signal on the Clk pin, the data are shifted one step forward. In a typical case, several L6372 are chained together. The clock signal is common. The Dout of the first is connected to the Din of the second, and so on, so that the external processor can, with a single shift operation, read the data of all the devices chained together, from the output Dout of the last in the chain.

RESET

An internal reset signal is generated any time an anomalous condition is detected, and used to block the device operation.
Such reset signal is generated when one (or both) of the following conditions is detected:

- undervoltage
- overtemperature

It inhibits the serial output, resets the shift register and the digital filters, but has no effect on the creation of the reference voltages of the internal comparators, nor on the continuous operation of the oscillator.
The reset disappears one or two clock pulses after the overtemperature or undervoltage condition has disappeared.

UNDERVOLTAGE DETECTION

The supply voltage is expected to range from 12V to 30V, even if its reference value is considered to be 24V.
In this range the L6372 operates correctly. Below 12V the overall system has to be considered not reliable. Consequently the supply voltage is monitored continuously and a signal, called UV, is internally generated and used.
The signal is "on" as long as the supply voltage does not reach the upper internal threshold of the V_s comparator (called V_{sh} and typically found at 10.4V). The UV disappears above V_{sh}.
Once the UV has been removed, the supply voltage must decrease below the lower threshold (called V_{sl}, and typically set at 10.2V) before it is turned on again.
The hysteresis of approximately 800mV is provided to prevent intermittent operation of the device at low supply voltages that may have a superimposed ripple around the average value.

OVERTEMPERATURE

If the chip temperature exceeds T_h (measured in a central position in the chip) the chip deactivates itself, because an internal signal, called OT, forces the reset signal. To reduce the device power dissipation to a minimum, the OT signal turns-off the internal current generators of the eight channels and the internal oscillator operations. Normal condition (OT low) is resumed as soon as (typically after some seconds) the chip temperature monitored goes back below T_l.
The different thresholds T_h and T_l, with hysteretic behavior, assure that no intermittent conditions can be generated.
Typical values for T_h and T_l, are 170°C and 150°C.

Figure 8: Timing

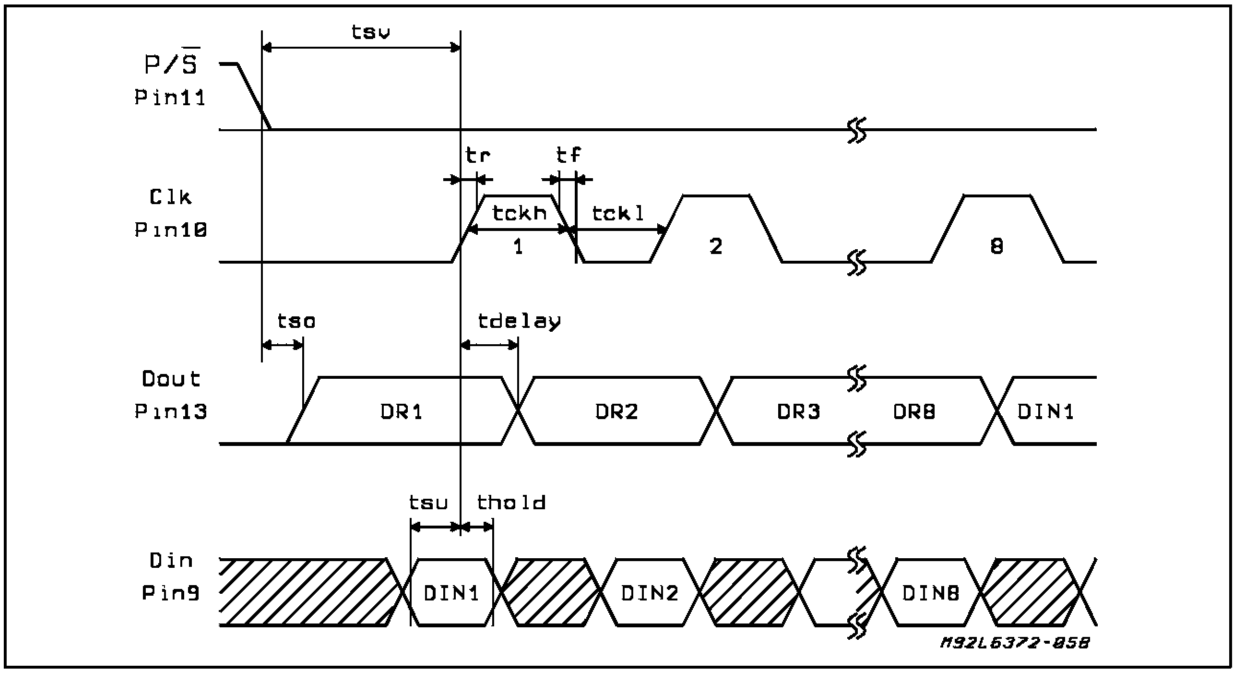
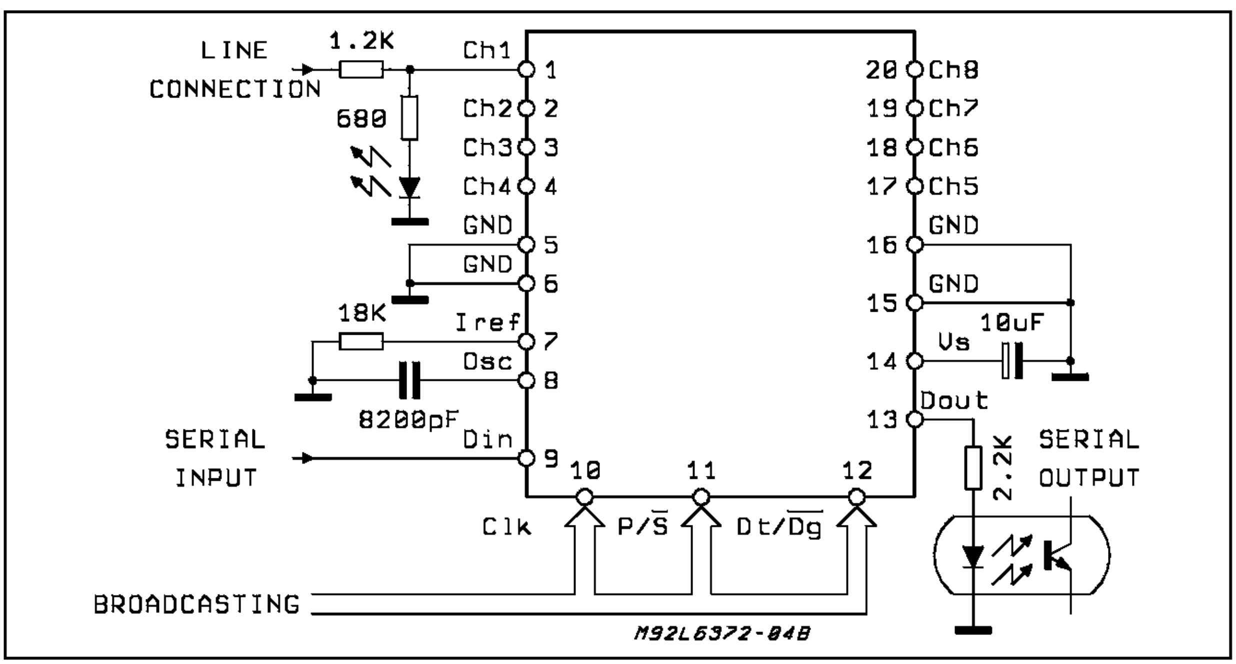
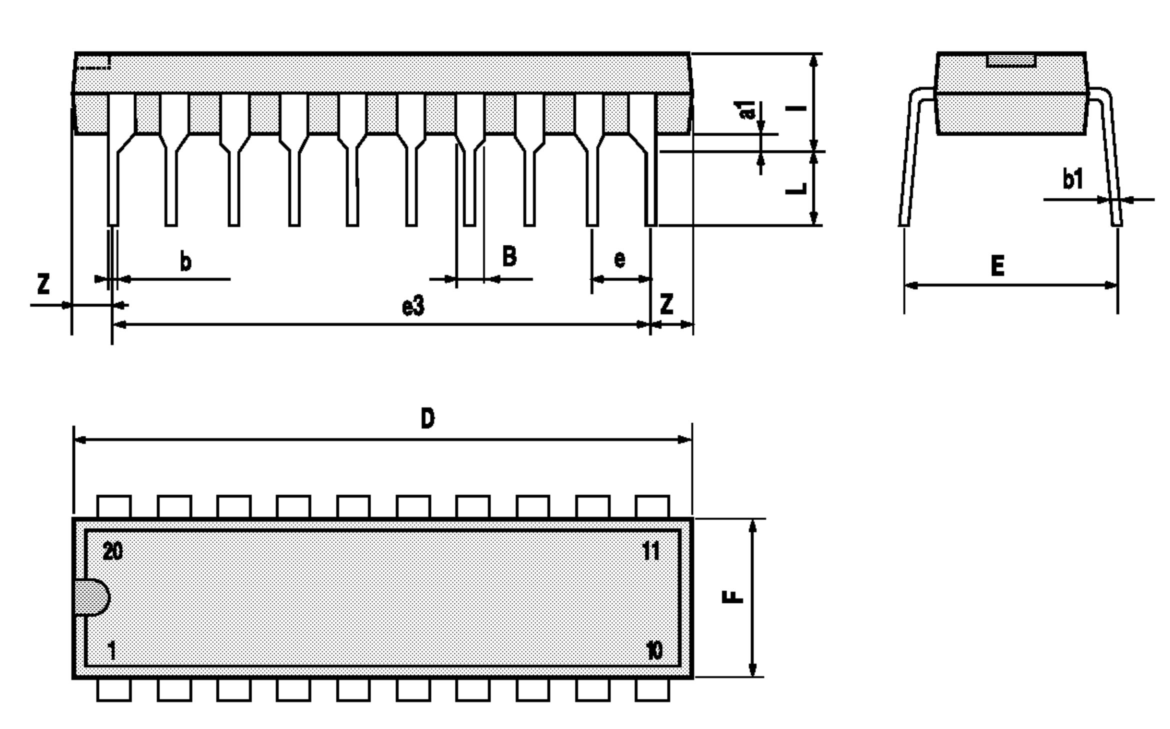


Figure 9: Typical Application



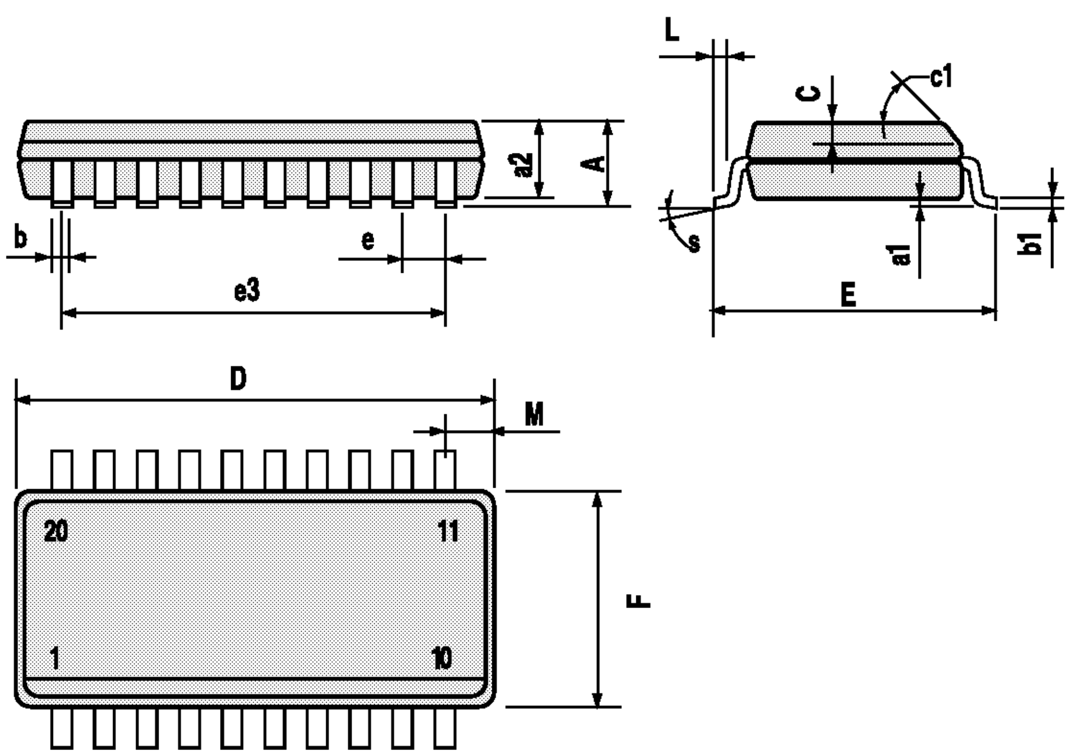
POWERDIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					



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